These schematics / code / layouts are for the Skywave H1 Pitch-only “Theremin”. 16 of these were built and operated in the Royal Festival Hall (South-bank arts centre) for 10 days in 2010.

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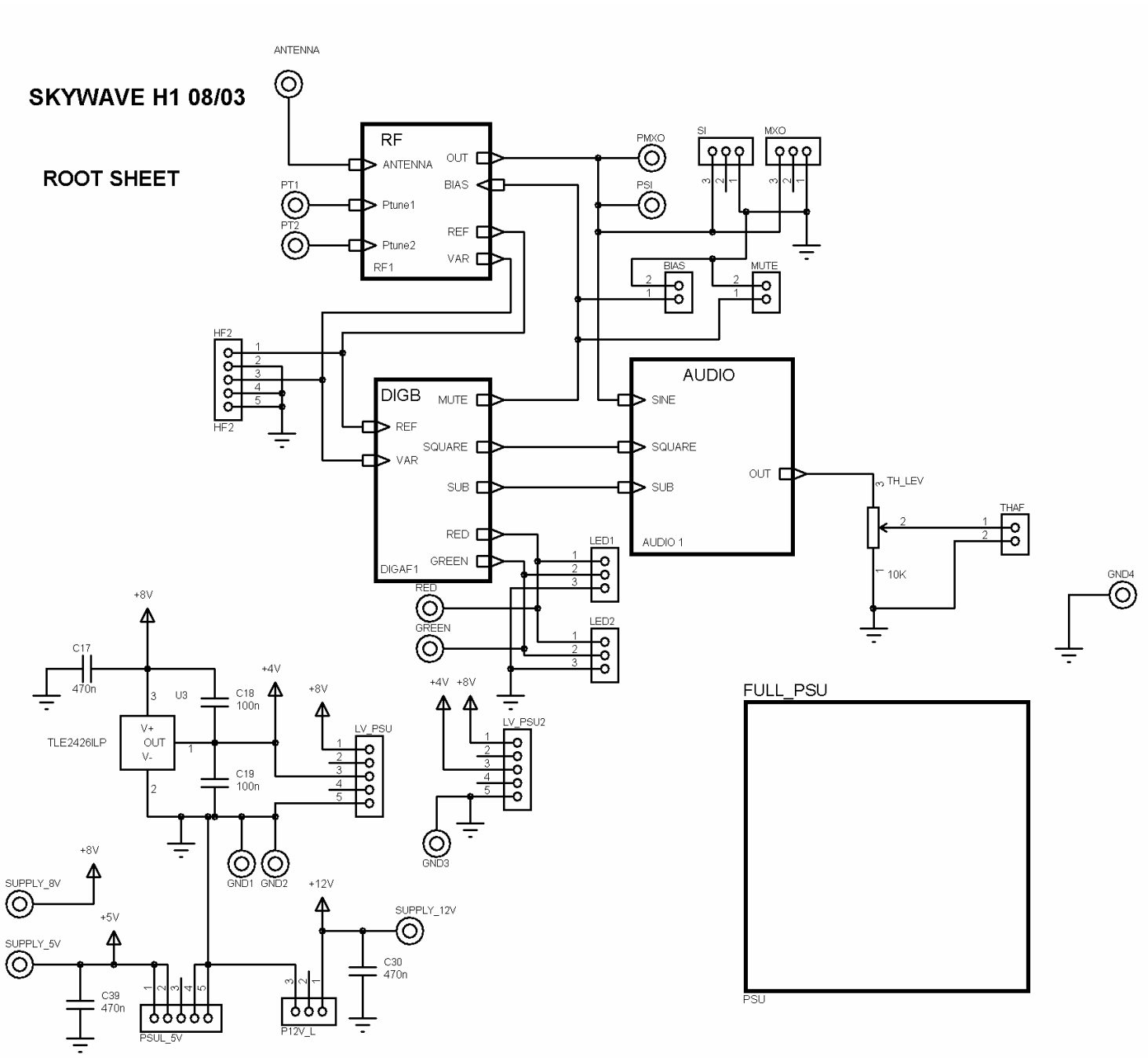
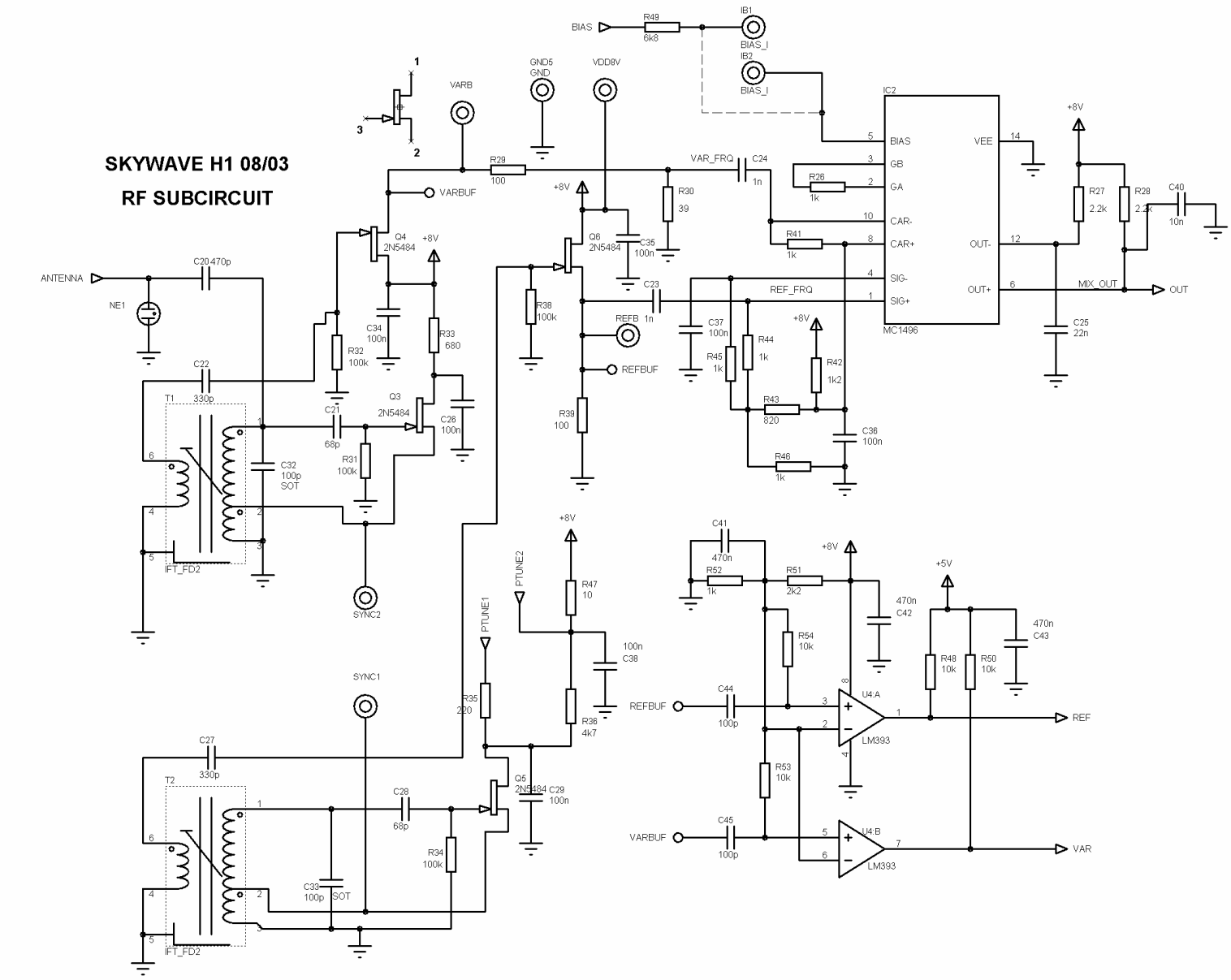
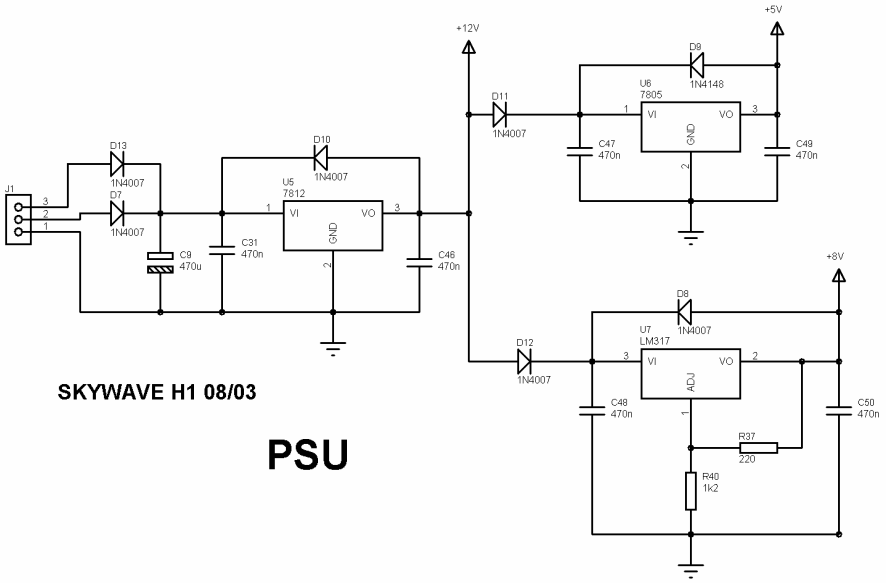
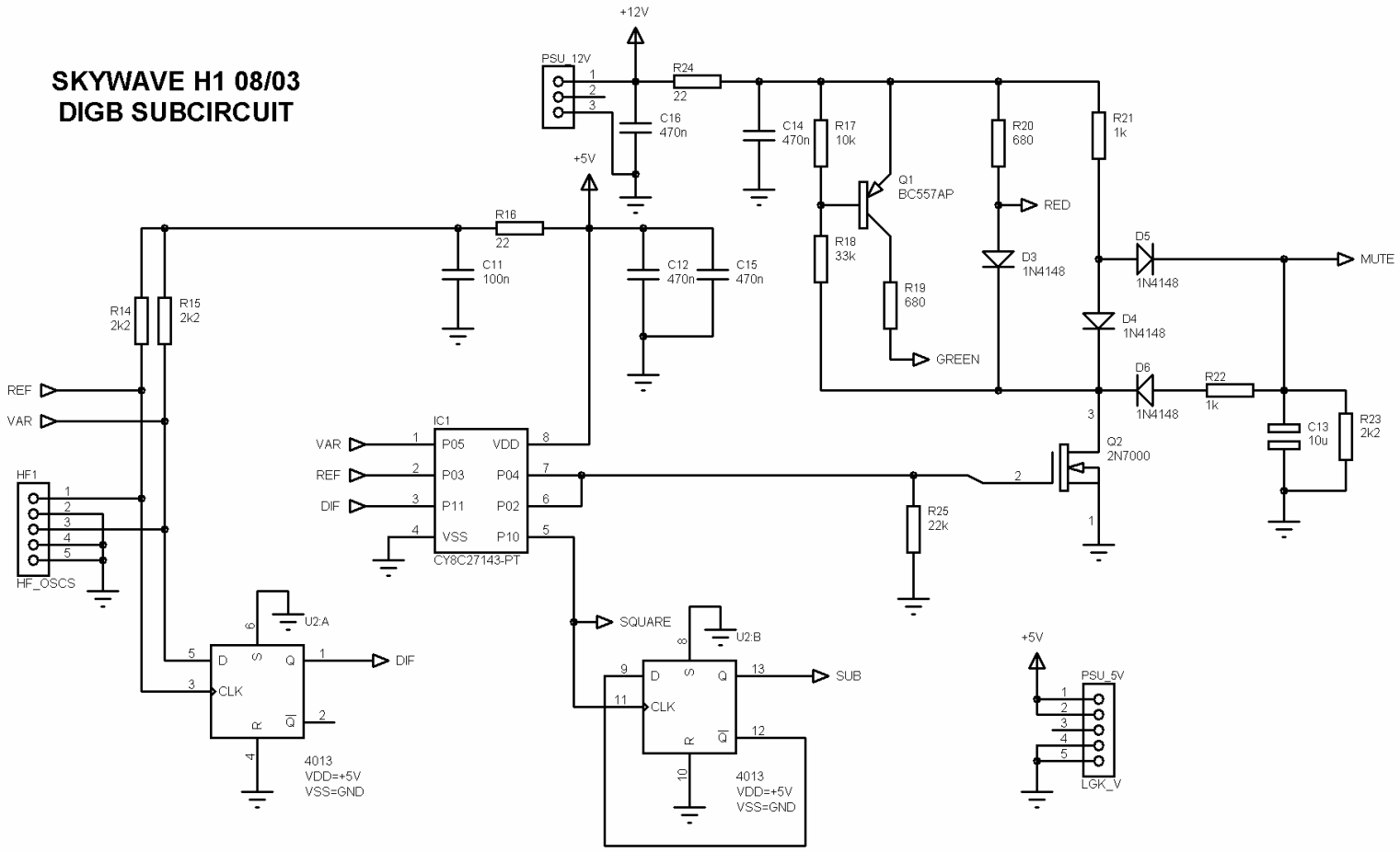
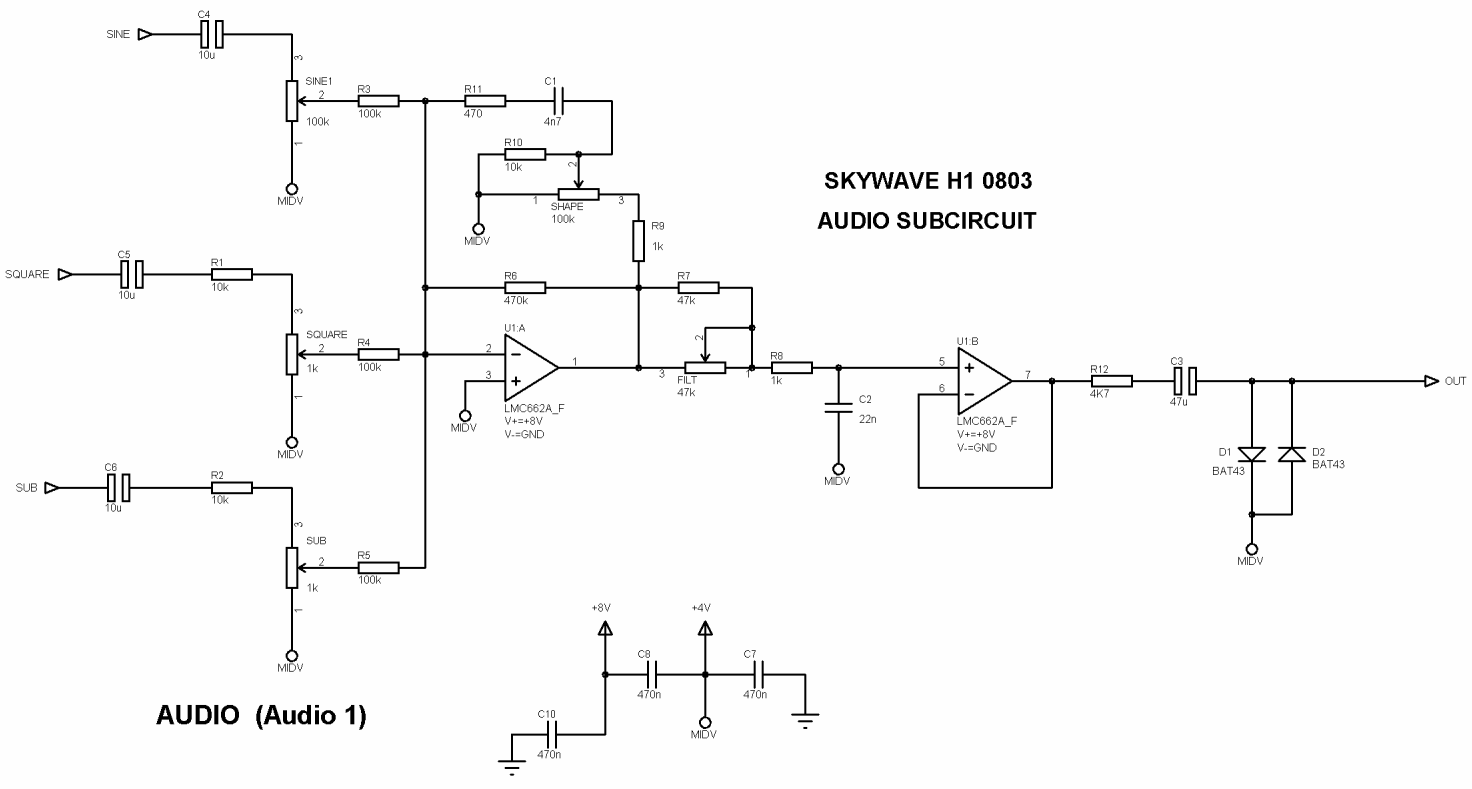



SKYWAVE H1 08/03
RF SUBCIRCUIT
BIAS
R48
6k8
IB1
BIAS_I
IB2
BIAS_I
GND5
GND
VDD8V
VARB
VARBUF
R29
100
VAR_FRQ
C24
1n
R30
39
+8V
IC2
BIAS
GB
GA
CAR-
CAR+
SIG-
SIG+
VEE
OUT-
OUT+
MC1496
R26
1k
R41
1k
REF_FRQ
C23
1n
REFB
REFBUF
R27
2.2k
R28
2.2k
C40
10n
MIX_OUT
OUT
C25
22n
ANTENNA
NE1
C20 470p
Q4
2N5484
Q6
2N5484
C35
100n
C34
100n
R32
100k
R33
680
R38
100k
C22
T1
330p
C21
68p
Q3
2N5484
C26
100n
R31
100k
C32
100p
SOT
IFT_FD2
SYNC2
R39
100
C37
100n
R45
1k
R44
1k
R42
1k2
R43
820
C36
100n
R46
1k
PTUNE2
PTUNE1
R47
10
C38
100n
R35
220
R36
4k7
SYNC1
C27
330p
T2
C28
68p
Q5
2N5484
C29
100n
R34
100k
C33
100p
SOT
IFT_FD2
C41
470n
R52
1k
R51
2k2
C42
470n
R54
10k
R53
10k
C44
100p
C45
100p
REFBUF
VARBUF
U4:A
U4:B
LM393
LM393
R48
10k
R50
10k
C43
470n
REF
VAR


SKYWAVE H1 08/03
PSU
+12V
+5V
+8V
D13
1N4007
D7
1N4007
D10
1N4007
U5
7812
J1
C9
470u
C31
470n
C46
470n
D9
1N4148
D11
1N4007
U6
7805
C47
470n
C49
470n
D8
1N4007
D12
1N4007
U7
LM317
ADJ
C48
470n
C50
470n
R37
220
R40
1k2


SKYWAVE H1 08/03
DIGB SUBCIRCUIT
+12V
PSU_12V
R24
22
C16
470n
+5V
C14
470n
R17
10k
Q1
BC557AP
R18
33k
R19
680
GREEN
R20
680
RED
D3
1N4148
R21
1k
D5
1N4148
MUTE
D4
1N4148
D6
1N4148
R22
1k
C13
10u
R23
2k2
Q2
2N7000
R25
22k
R16
22
C11
100n
C12
470n
C15
470n
R14
2k2
R15
2k2
REF
VAR
HF1
HF_OSCS
IC1
P05
P03
P11
VSS
VDD
P04
P02
P10
CY8C27143-PT
SQUARE
DIF
U2:A
U2:B
4013
VDD=+5V
VSS=GND
SUB
PSU_5V
LGK_V


SKYWAVE H1 0803
AUDIO SUBCIRCUIT
SINE
SQUARE
SUB
C4
10u
C5
10u
C6
10u
SINE1
SQUARE
SUB
100k
1k
1k
R3
100k
R4
100k
R5
100k
R11
470
C1
4n7
R10
10k
SHAPE
100k
R9
1k
R1
10k
R2
10k
R6
470k
R7
47k
FILT
47k
R8
1k
C2
22n
U1:A
U1:B
LMC662A_F
V+=+8V
V-=GND
R12
4K7
C3
47u
OUT
D1
BAT43
D2
BAT43
MIDV
+8V
+4V
C8
470n
C7
470n
C10
470n
AUDIO (Audio 1)

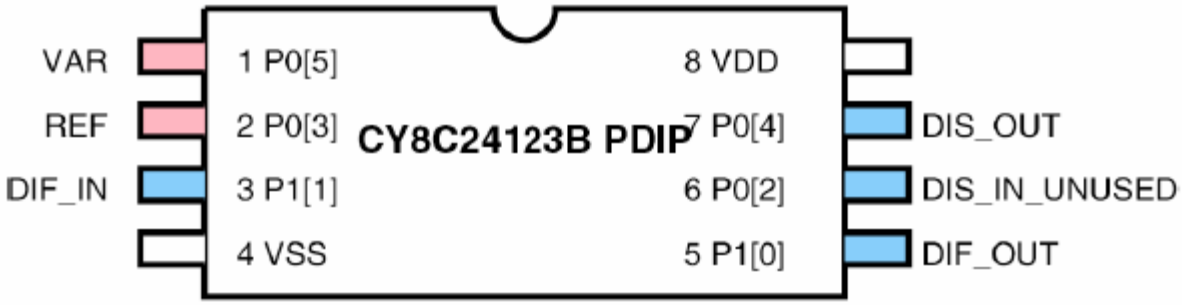
I can provide a pre-programmed H1 PSoC for £15. Email : fred@fundes.co.uk
All code and details required to copy this part are provided below, and PSoC designer is available from Cypress FOC.

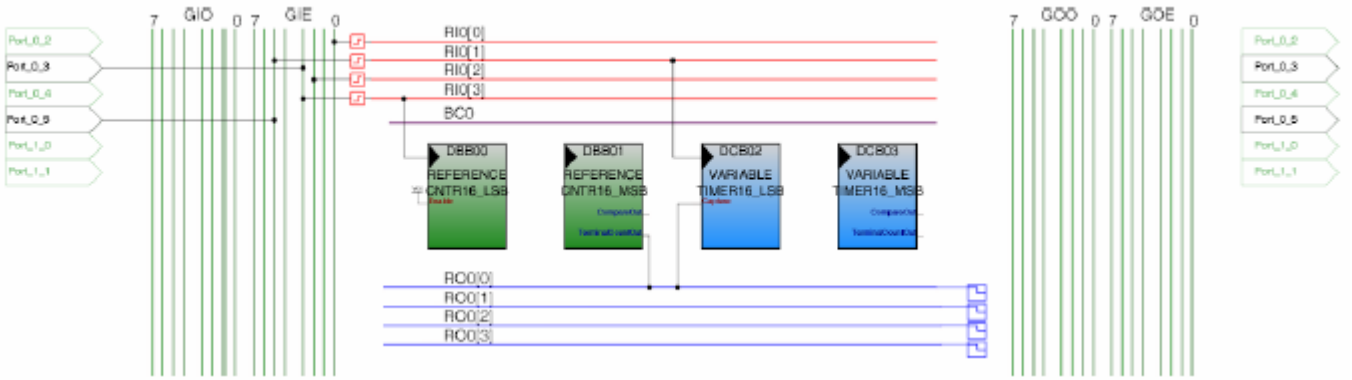
Configuration of PSoC CY8C27143: IC 1

Extremely simple – Frequencies of reference and variable oscillators are compared using the CTR16 and TIMER16 UM's, The state is computed in the UM's ISR's (Interrupt Service Routines) and these return a flag (Null) which is polled by the main routine – If Variable oscillator frequency exceeds Reference oscillator frequency, Null is set, P0:4 is driven high, and the input on P1:1 is not passed through to P1:0

When Variable oscillator frequency < Reference oscillator frequency, Null is cleared, P0:4 is driven low, and the input on P1:1 is passed through to P1:0

It should be noted that this instrument has both analogue and "digital" signal paths, the "digital" signal path is disconnected by this PSoC when nulling (silencing) is required, the analogue signal is nulled at the mixer via the output from P0:4 (which also drives the LED).





Signal Pin Table (sky_h1_v2)

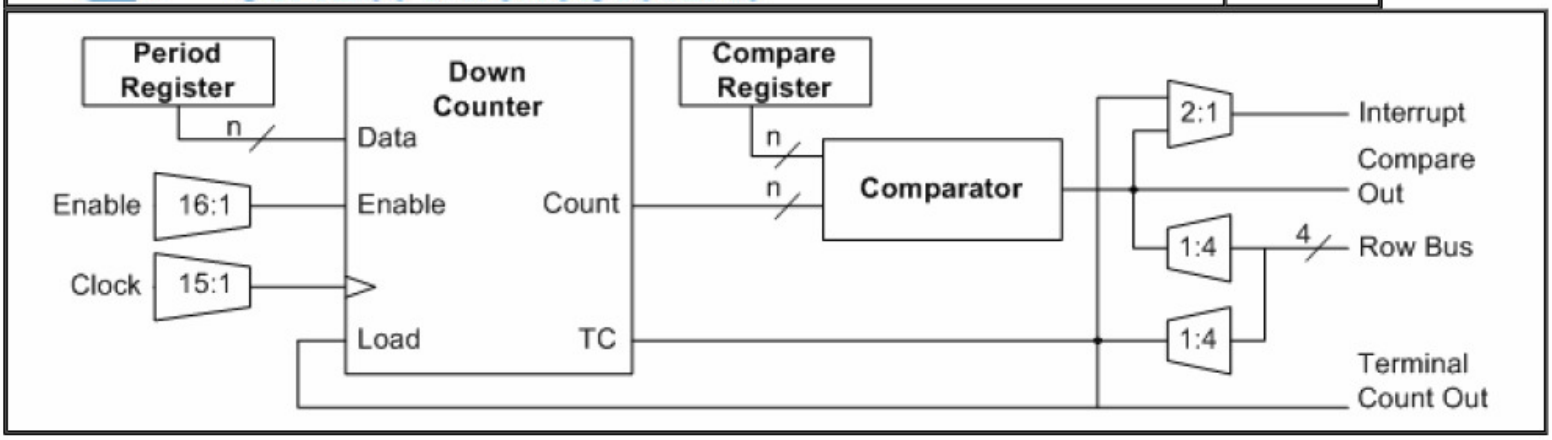
Pin #	Port	Label	Select	Drive	Interrupt
1	P0[5]	VAR	GlobalInEven_5	High Z	DisableInt
2	P0[3]	REF	GlobalInEven_3	High Z	DisableInt
3	P1[1]	DIF_IN	StdCPU	High Z	DisableInt
4	VSS				
5	P1[0]	DIF_OUT	StdCPU	Strong Slow	DisableInt
6	P0[2]	DIS_IN_UNUSED	StdCPU	High Z	DisableInt
7	P0[4]	DIS_OUT	StdCPU	Strong Slow	DisableInt
8	VDD				

Selected Global Parameters (sky_h1_v2)

Name	Value
32K_Select	Internal
A_Buff_Power	Low
Analog Power	All Off
CPU_Clock	SysClk/1
LVDThrottleBack	Disable
Op-Amp Bias	Low
PLL_Mode	Disable
Power Setting [Vcc / SysClk freq]	5.0V / 24MHz
Ref Mux	(Vdd/2)+/-BandGap
Sleep_Timer	512_Hz
SwitchModePump	OFF
SysClk*2 Disable	Yes
Trip Voltage [LVD (SMP)]	4.81V (5.00V)
VC1= SysClk/N	1
VC2= VC1/N	1
VC3 Divider	1
VC3 Source	SysClk/1
Watchdog Enable	Disable

User Module Detail REFERENCE
(Counter16)

CYPRESS MICROSYSTEMS



Parameters

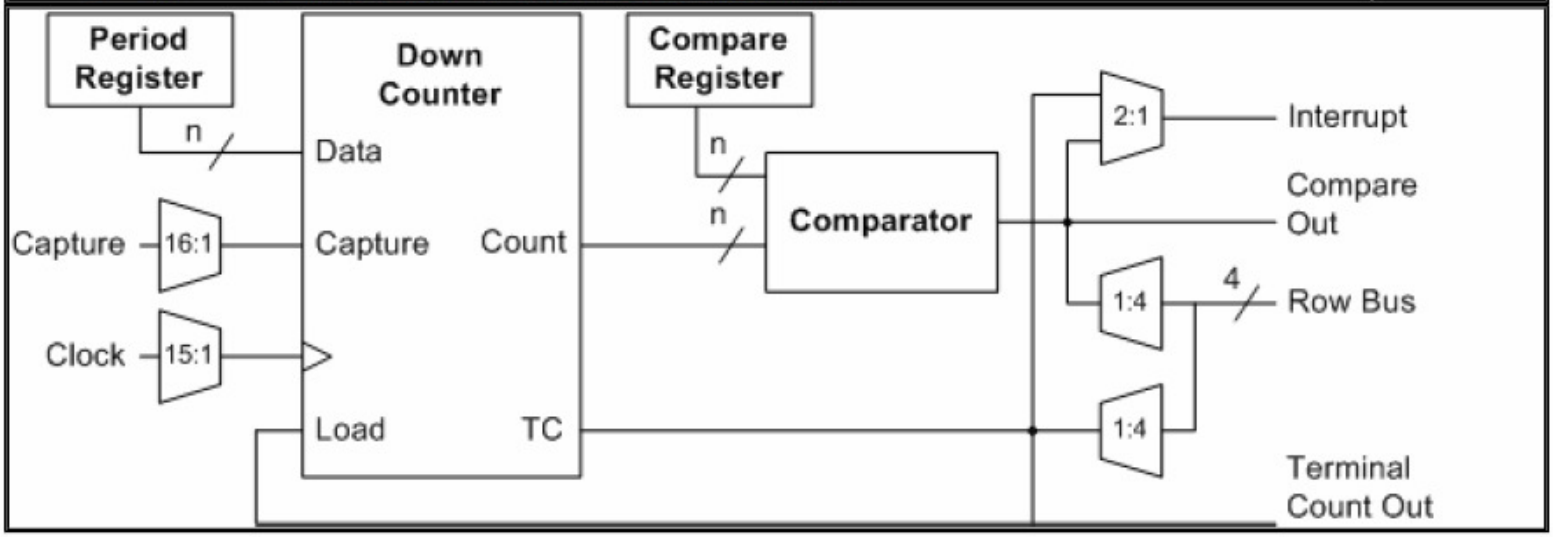
Parameters	Value
Clock	Row_0_Input_3
ClockSync	Unsynchronized
CompareOut	None
CompareType	Less Than
CompareValue	0000
Enable	High
IntDispatchMode	ActiveStatus
InterruptAPI	Enable
InterruptType	Terminal Count
InvertEnable	Normal
Period	65535
TerminalCountOut	Row_0_Output_0

Blocks

Block	Type	Location	
CNTR16_LSB	DIGITAL	0	
Registers	**Name**	**Address**	**Value**
CONTROL_0	DBB00CR0	23	0
DATA_0	DBB00DR0	20	0
DATA_1	DBB00DR1	21	ff
DATA_2	DBB00DR2	22	0
DIG_BasicFunction	DBB00FN	120	11
DIG_Input	DBB00IN	121	1f
DIG_Output	DBB00OU	122	0
Block	**Type**	**Location**	
CNTR16_MSB	DIGITAL	1	
Registers	**Name**	**Address**	**Value**
CONTROL_0	DBB01CR0	27	0
DATA_0	DBB01DR0	24	0
DATA_1	DBB01DR1	25	ff
DATA_2	DBB01DR2	26	0
DIG_BasicFunction	DBB01FN	124	31
DIG_Input	DBB01IN	125	3f
DIG_Output	DBB01OU	126	20

User Module Detail VARIABLE (Timer16)

CYPRESS MICROSYSTEMS



Parameters

Parameters	Value
Capture	Row_0_Output_0
Clock	Row_0_Input_1
ClockSync	Unsynchronized
CompareOut	None
CompareType	Less Than Or Equal
CompareValue	0000
IntDispatchMode	ActiveStatus
InterruptAPI	Enable
InterruptType	Terminal Count
InvertCapture	Normal
Period	65535
TC_PulseWidth	Full Clock
TerminalCountOut	None

Blocks

Block	Type	Location	
TIMER16_LSB	DIGITAL	2	
Registers	**Name**	**Address**	**Value**
CONTROL_0	DCB02CR0	2b	0
DATA_0	DCB02DR0	28	0
DATA_1	DCB02DR1	29	ff
DATA_2	DCB02DR2	2a	0
DIG_BasicFunction	DCB02FN	128	0
DIG_Input	DCB02IN	129	8d
DIG_Output	DCB02OU	12a	0
Block	**Type**	**Location**	
TIMER16_MSB	DIGITAL	3	
Registers	**Name**	**Address**	**Value**
CONTROL_0	DCB03CR0	2f	4
DATA_0	DCB03DR0	2c	0
DATA_1	DCB03DR1	2d	ff
DATA_2	DCB03DR2	2e	0
DIG_BasicFunction	DCB03FN	12c	20
DIG_Input	DCB03IN	12d	3d
DIG_Output	DCB03OU	12e	0

Global Register Values (sky_h1_v2)

Register	Name	Address	Value
AnalogClockSelect1	CLK_CR1	161	0
AnalogClockSelect2	CLK_CR2	169	0
AnalogColumnClockSelect	CLK_CR0	160	0
AnalogColumnInputSelect	AMX_IN	60	9
AnalogComparatorControl1	CMP_CR1	66	0
AnalogIOControl_0	ABF_CR0	162	0
AnalogLUTControl0	ALT_CR0	167	33
AnalogLUTControl1	ALT_CR1	168	0
AnalogModulatorControl_0	AMD_CR0	163	0
AnalogModulatorControl_1	AMD_CR1	166	0
AnalogReferenceControl	ARF_CR	63	0
AnalogSyncControl	ASY_CR	65	0
DecimatorControl_0	DEC_CR0	e6	0
DecimatorControl_1	DEC_CR1	e7	0
GlobalDigitalInterconnect_Drive_Even_Input	GDI_E_IN	1d1	0
GlobalDigitalInterconnect_Drive_Even_Output	GDI_E_OU	1d3	0
GlobalDigitalInterconnect_Drive_Odd_Input	GDI_O_IN	1d0	0
GlobalDigitalInterconnect_Drive_Odd_Output	GDI_O_OU	1d2	0
I2CConfig	I2CCFG	d6	0
OscillatorControl_1	OSC_CR1	1e1	0
OscillatorControl_2	OSC_CR2	1e2	1
OscillatorControl_3	OSC_CR3	1df	0
OscillatorControl_4	OSC_CR4	1de	0
OscillatorGlobalBusEnableControl	OSC_GO_EN	1dd	0
Port_0_DriveMode_0	PRT0DM0	100	10

Port_0_DriveMode_1	PRT0DM1	101	2c
Port_0_DriveMode_2	PRT0DM2	3	10
Port_0_GlobalSelect	PRT0GS	2	28
Port_0_IntCtrl_0	PRT0IC0	102	0
Port_0_IntCtrl_1	PRT0IC1	103	0
Port_0_IntEn	PRT0IE	1	0
Port_1_DriveMode_0	PRT1DM0	104	1
Port_1_DriveMode_1	PRT1DM1	105	2
Port_1_DriveMode_2	PRT1DM2	7	1
Port_1_GlobalSelect	PRT1GS	6	0
Port_1_IntCtrl_0	PRT1IC0	106	0
Port_1_IntCtrl_1	PRT1IC1	107	0
Port_1_IntEn	PRT1IE	5	0
Port_2_DriveMode_0	PRT2DM0	108	0
Port_2_DriveMode_1	PRT2DM1	109	0
Port_2_DriveMode_2	PRT2DM2	b	0
Port_2_GlobalSelect	PRT2GS	a	0
Port_2_IntCtrl_0	PRT2IC0	10a	0
Port_2_IntCtrl_1	PRT2IC1	10b	0
Port_2_IntEn	PRT2IE	9	0
Row_0_InputMux	RDI0RI	b0	4
Row_0_InputSync	RDI0SYN	b1	0
Row_0_LogicInputAMux	RDI0IS	b2	0
Row_0_LogicSelect_0	RDI0LT0	b3	33
Row_0_LogicSelect_1	RDI0LT1	b4	33
Row_0_OutputDrive_0	RDI0SRO0	b5	0
Row_0_OutputDrive_1	RDI0SRO1	b6	0

```
//-------------------------------------------------------------------------
// C main line
//-------------------------------------------------------------------------

#include <m8c.h>        // part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

unsigned int captured;
unsigned int last_captured;
unsigned int calculated;
unsigned int temp;
unsigned char ovflow;
unsigned char nullctr;
unsigned char null;
```

```
#define M_READ_DIF      PRT1DR&0x02
#define SET_DIF    PRT1DR=1
#define CLR_DIF    PRT1DR=0
#define CLR_NULL_to_LOW PRT0DR=0
#define SET_NULL_to_HIGH PRT0DR=0x10

#define REFTICKS 32000


void main()
{

REFERENCE_WritePeriod(REFTICKS);
VARIABLE_WritePeriod(0xFFFF);
last_captured = 0xFFFF;

REFERENCE_EnableInt();
VARIABLE_EnableInt();

M8C_EnableGInt;

REFERENCE_Start();
VARIABLE_Start();

while(1)
        {
        if(null==0)
                {
                if(M_READ_DIF)
                        SET_DIF;
                else CLR_DIF;
                }
        }
}

//=========================================================================================
=

#pragma interrupt_handler REFERENCE_ISR
void REFERENCE_ISR(void)
{
captured = VARIABLE_wReadCompareValue();
//-------------------------------------------------
if(ovflow < 2)
        {
        ovflow = 0;
        //-------------------------------------------------
        if(captured > last_captured)
                {
                calculated = last_captured;
                temp = 0xFFFF - captured;
                calculated = calculated+temp;

                if(calculated >= REFTICKS)
```

```
                {

                if(nullctr < 2)
                        nullctr++;
                }
        else if(nullctr > 0)
                nullctr--;
        }
        //-----------------------------------------------
    else{
        calculated = (last_captured - captured);
        if(calculated >= REFTICKS)
                {
                if(nullctr < 2)
                        nullctr++;
                }
        else if(nullctr > 0)
                        nullctr--;
        }
        //-----------------------------------------------

        if(nullctr == 2)
                {
                null = 1;
                SET_NULL_to_HIGH;
                }
        else if(nullctr == 0)
                {
                null = 0;
                CLR_NULL_to_LOW;
                }
        //-----------------------------------------------
    }
else{       // ERROR HANDLER
    if(nullctr < 2)
        nullctr++;
    if(nullctr == 2)
        {
        null = 1;
        SET_NULL_to_HIGH;
        }
    }
last_captured = captured;
ovflow = 0;

}

//=============================================================================
=

#pragma interrupt_handler VARIABLE_ISR
void VARIABLE_ISR(void)
{
ovflow++;
}
```

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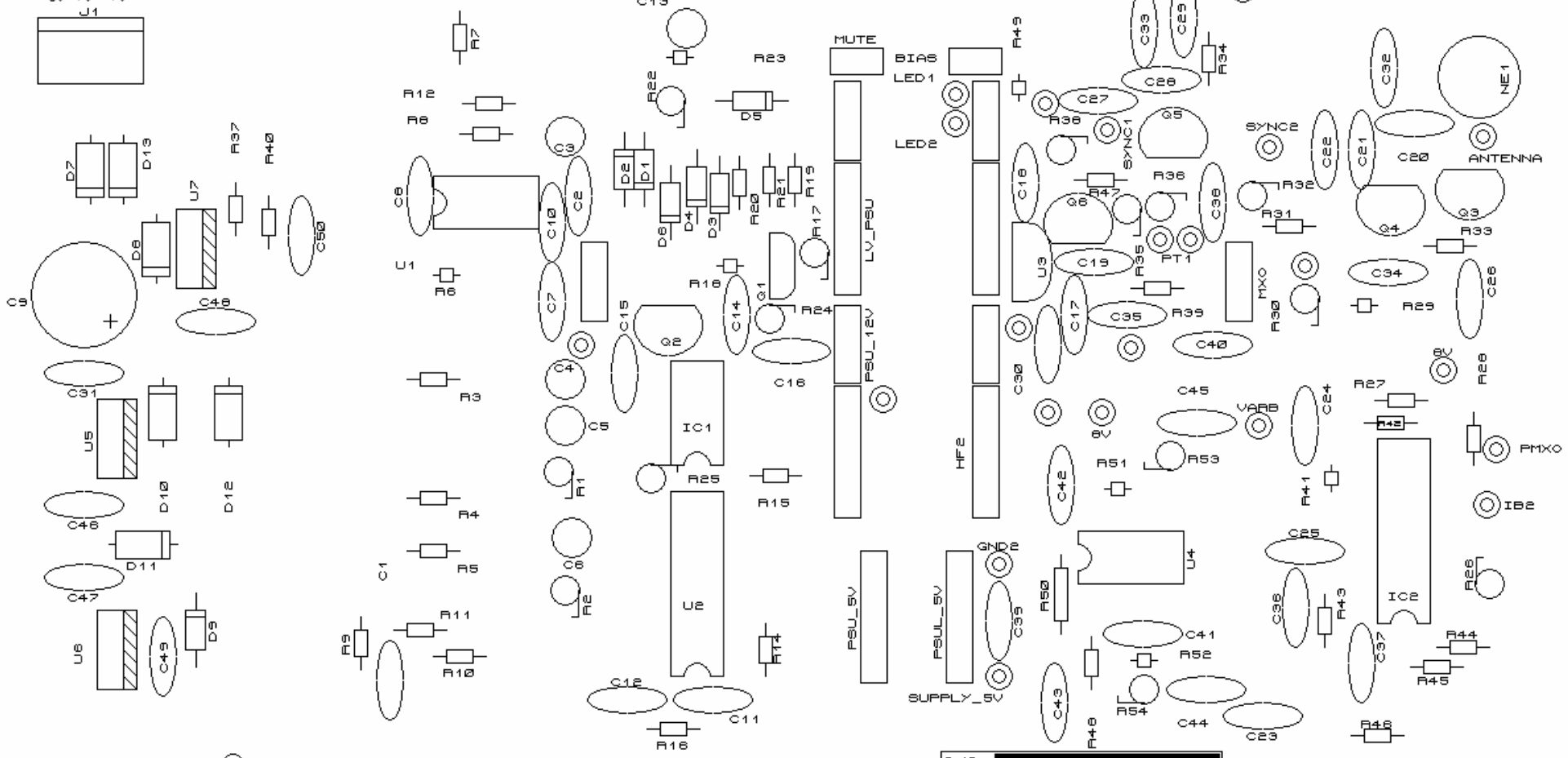
SkyWave "Hydrogen" H1 Pitch Board

Version 1.0 March 2010

Assy	Special	E-Test	L-Test	Signoff

Modifications:

Supply - Min 12VDC Max 24VDC
Or AC 24V CT to 0V Max
0V +V +V



Ref Frq:

Other:

SkyWave®
Theremins

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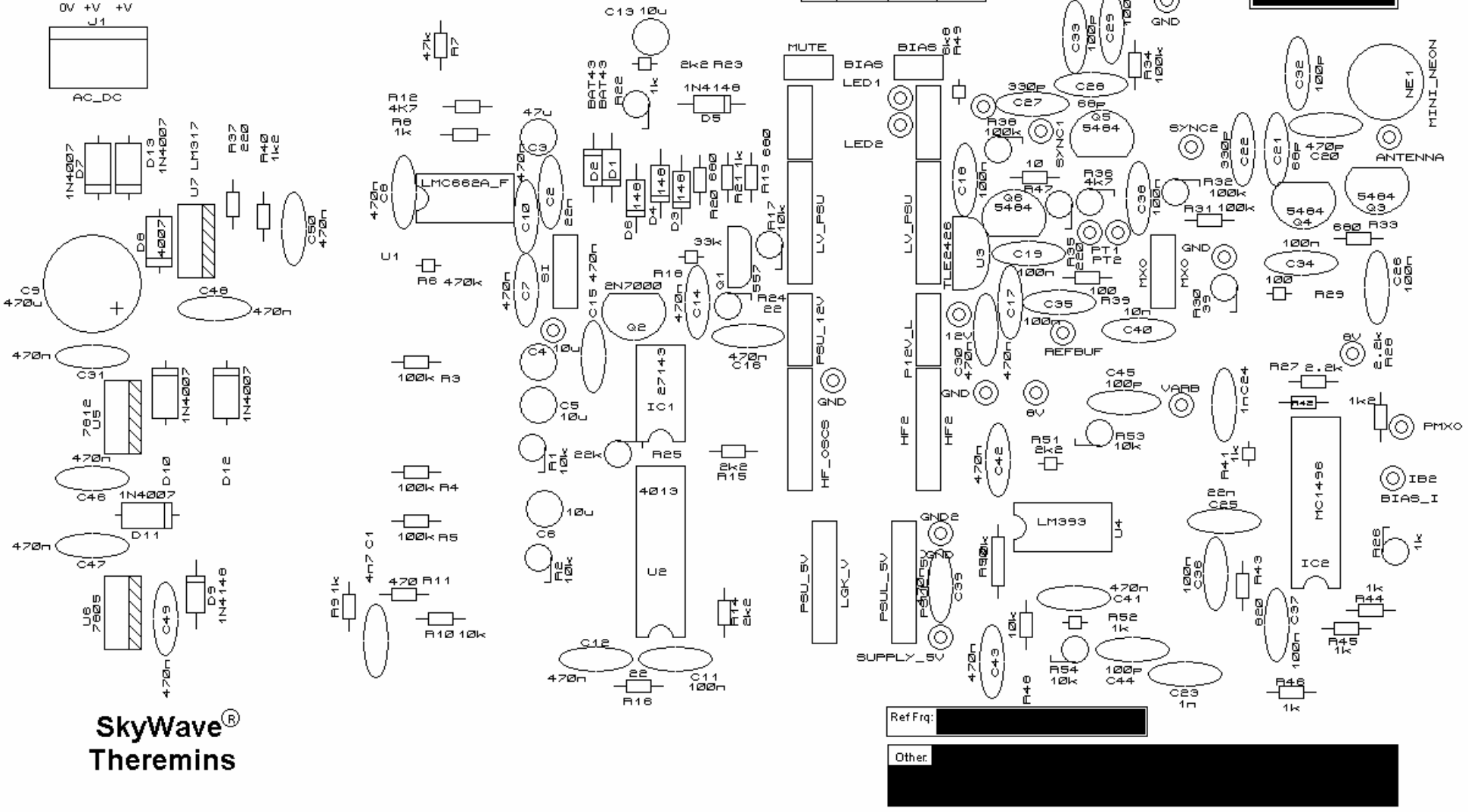
SkyWave "Hydrogen" H1 Pitch Board

Version 1.0 March 2010

Assy	Special	E-Test	L-Test	Signoff
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]

Modifications: [redacted]

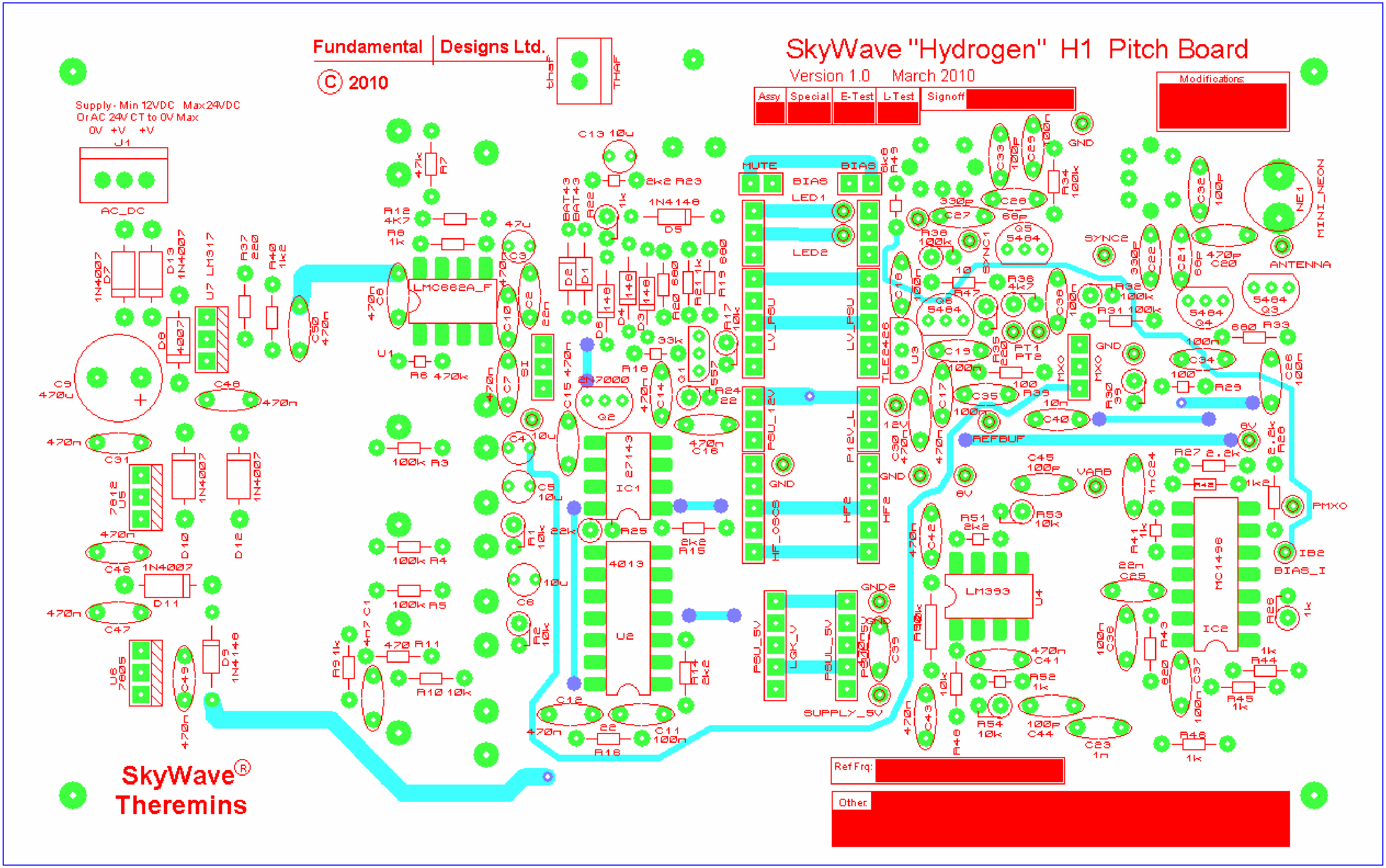
Supply - Min 12VDC Max 24VDC
Or AC 24V CT to 0V Max
0V +V +V



Ref Frq: [redacted]

Other: [redacted]

SkyWave®
Theremins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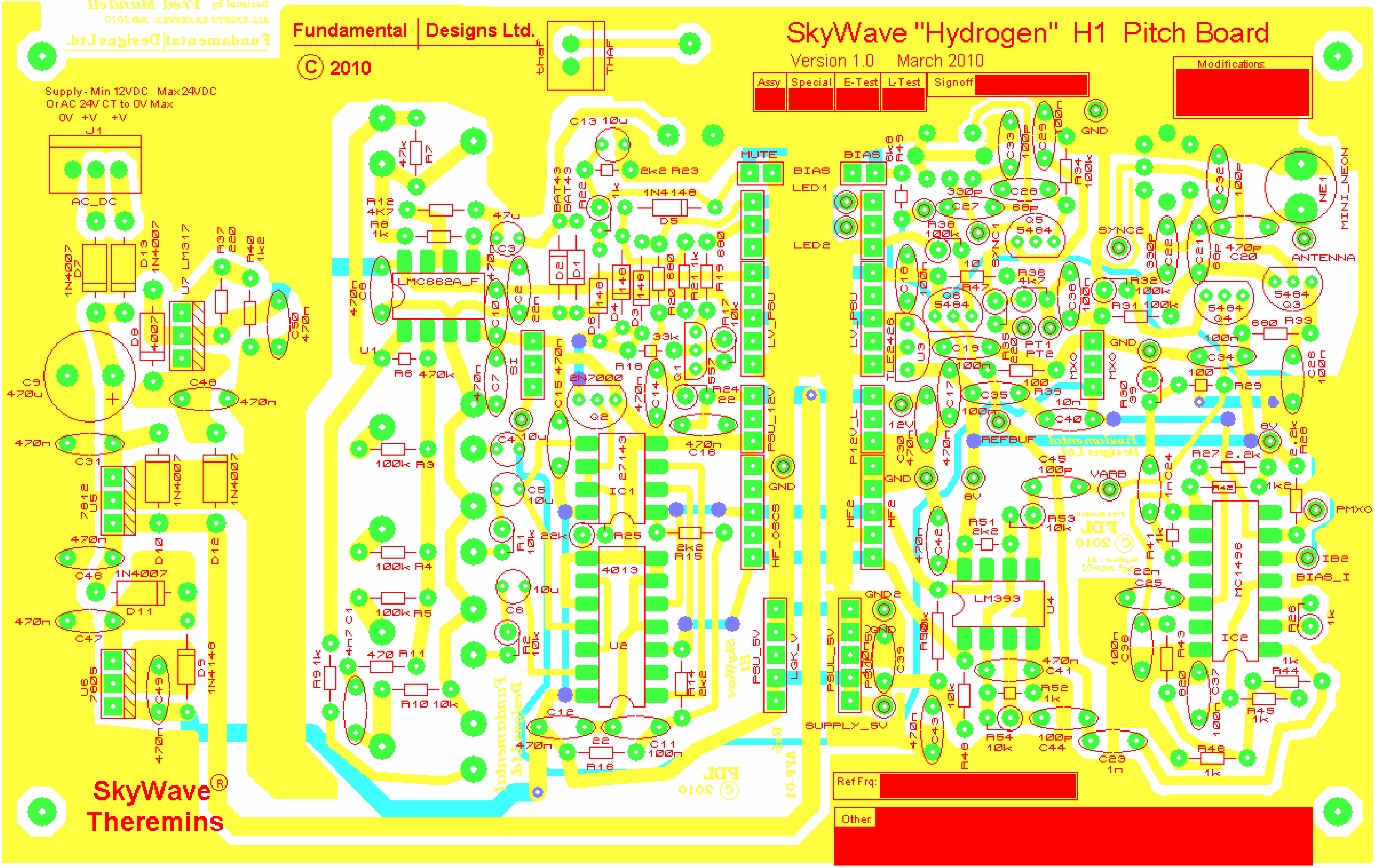
SkyWave "Hydrogen" H1 Pitch Board
Version 1.0 March 2010
Assy
Special
E-Test
L-Test
Signoff
Modifications
Supply - Min 12VDC Max 24VDC
Or AC 24V CT to 0V Max
0V +V +V
J1
AC_DC
Ref Frq:
Other
SkyWave®
Theremins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Assy
Special
E-Test
L-Test
Signoff
Modifications
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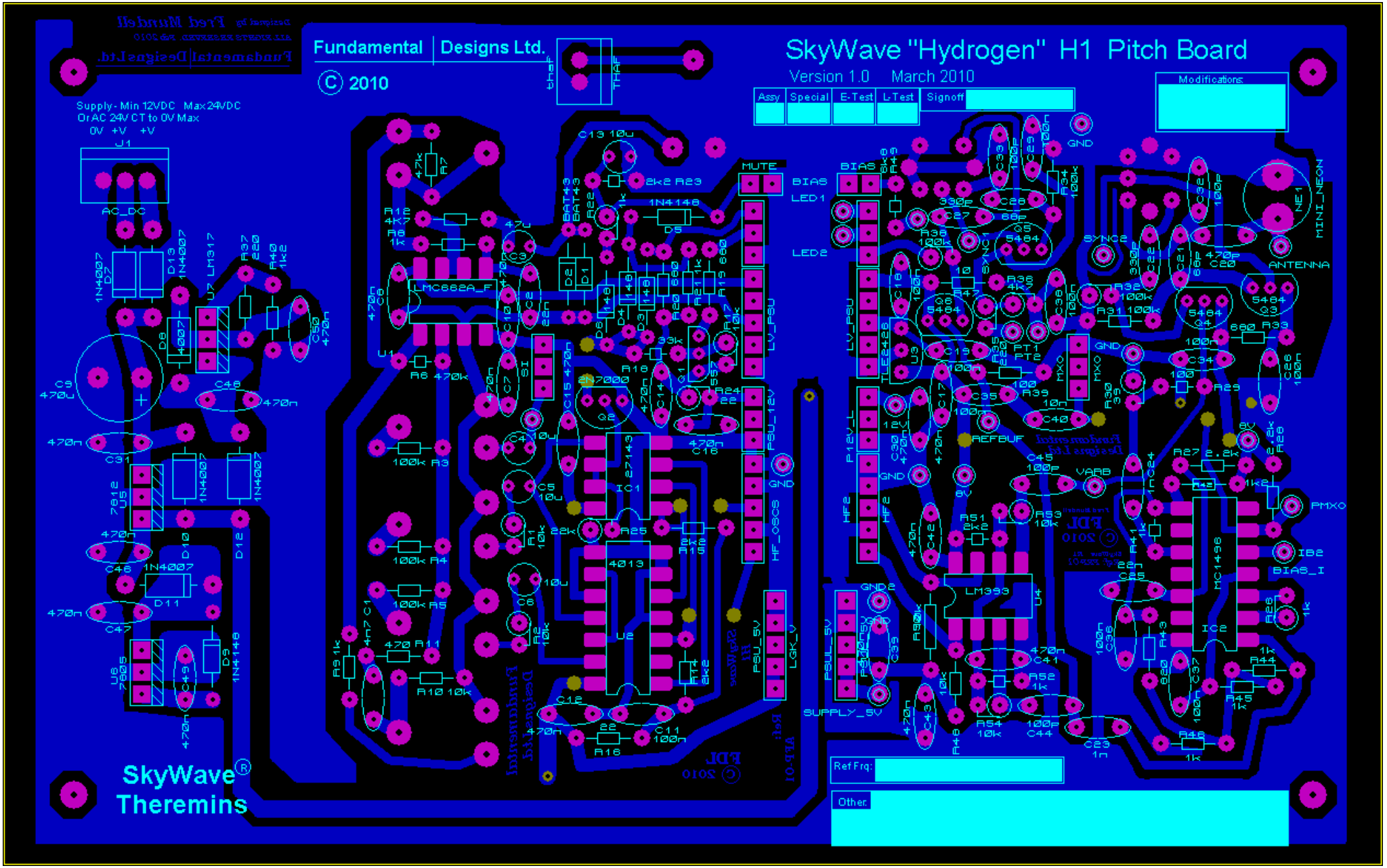
Supply - Min 12VDC Max 24VDC
Or AC 24V CT to 0V Max
0V +V +V
J1
AC_DC
Ref Frq:
Other
SkyWave®
Theremins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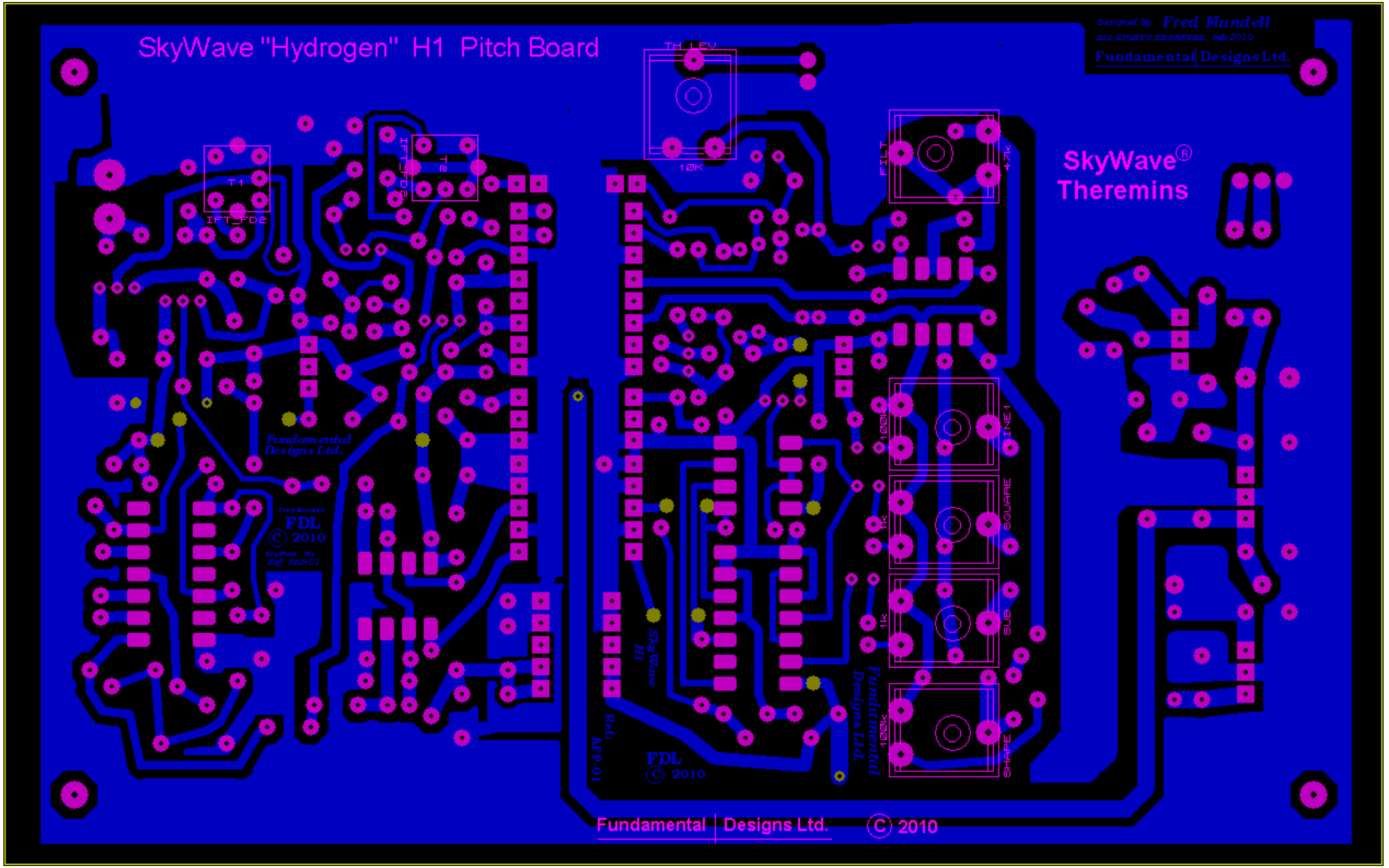
SkyWave "Hydrogen" H1 Pitch Board
Version 1.0 March 2010
Assy
Special
E-Test
L-Test
Signoff
Modifications
Supply - Min 12VDC Max 24VDC
Or AC 24V CT to 0V Max
0V +V +V
J1
AC_DC
LM1117
LM7812
LM7805
LM6882A_F
2N7000
4013
LM393
MC1496
TLE4266
MUTE
BIAS
LED1
LED2
HF_OSCS
LV_PSU
PSU_12V
PSU_5V
SUPPLY_5V
GND
GND2
REFBUF
VARB
PMXO
IBE
BIAS_I
SYNC1
SYNC2
MINI_NEON
ANTENNA
Ref Frq:
Other
SkyWave®
Theremins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Designed by Fred Mundell
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Fundamental Designs Ltd.
SkyWave®
Theremins
TH_FV
10K
T1
IFT_FD2
T2
IFT_FD1
FILT
47k
100k
LINE1
1k
SQUARE
SUB
SHAPE
Fundamental
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SkyWave H1
Ref: XXP-01
Ref: AFP-10
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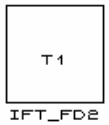
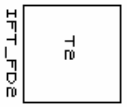
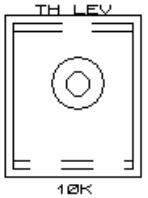
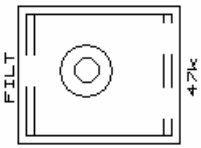
SkyWave "Hydrogen" H1 Pitch Board









SkyWave® Theremins